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12 June 2007 NSA/0583(2007)-C3/4213

STANAG 4213 C3 (EDITION 3) – THE NATO MULTI-CHANNEL TACTICAL DIGITAL GATEWAY - CIRCUIT SWITCHED DATA TRANSMISSION STANDARDS –

References:

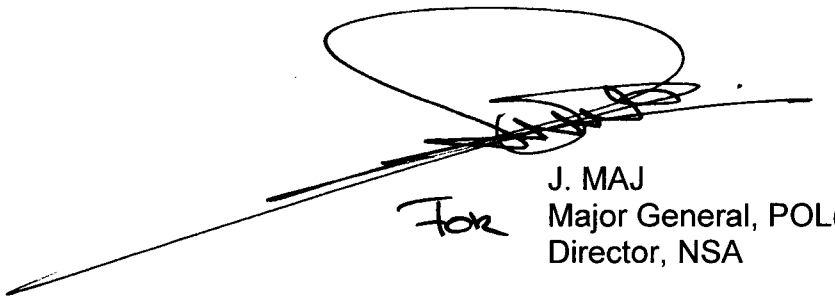
a. MAS/412-EL/4213 dated 15 November 1993 (Edition 2)
b. AC322(SC6)N/89, dated 4 September 1998 – Ratification Request (Edition 3)

1. The enclosed NATO Standardization Agreement, which has been ratified by nations as reflected in the **NATO Standardization Document Database (NSDD)**, is promulgated herewith.

2. The references listed above are to be destroyed in accordance with local document destruction procedures.

ACTION BY NATIONAL STAFFS

3. National staffs are requested to examine their ratification status of the STANAG and, if they have not already done so, advise the NHQC3S, through their national delegation as appropriate of their intention regarding its ratification and implementation.



J. MAJ
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Enclosure:
STANAG 4213 (Edition 3)

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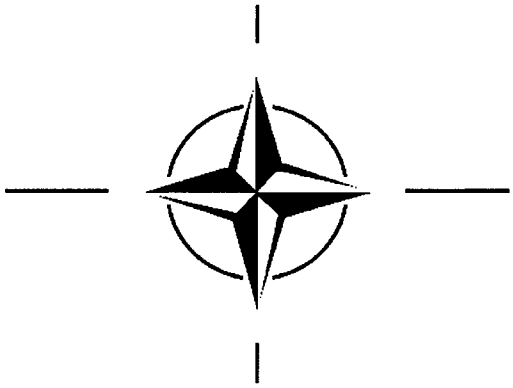
STANAG 4213
(Edition 3)

NORTH ATLANTIC TREATY ORGANIZATION
(NATO)



NATO STANDARDIZATION AGENCY
(NSA)

STANDARDIZATION AGREEMENT
(STANAG)

SUBJECT: **THE NATO MULTI-CHANNEL TACTICAL DIGITAL GATEWAY - CIRCUIT SWITCHED DATA TRANSMISSION STANDARDS -**

Promulgated on 12 June 2007

J. MAJ
Major General, POL(A)
Director, NSA

STANAG 4213
(Edition 3)

RECORD OF AMENDMENTS

No.	Reference/date of Amendment	Date Entered	Signature

EXPLANATORY NOTES

AGREEMENT

1. This NATO Standardization Agreement (STANAG) is promulgated by the Director NATO Standardization Agency under the authority vested in him by the NATO Standardization Organisation Charter.

2. No departure may be made from the agreement without informing the tasking authority in the form of a reservation. Nations may propose changes at any time to the tasking authority where they will be processed in the same manner as the original agreement.

3. Ratifying nations have agreed that national orders, manuals and instructions implementing this STANAG will include a reference to the STANAG number for purposes of identification.

RATIFICATION, IMPLEMENTATION AND RESERVATIONS

4. Ratification, implementation and reservation details are available on request or through the NSA websites (internet http://nsa.nato.int; NATO Secure WAN http://nsa.hq.nato.int).

FEEDBACK

5. Any comments concerning this publication should be directed to NATO/NSA – Bvd Leopold III - 1110 Brussels - BE.

STANAG 4213
(Edition 3)

NATO STANDARDIZATION AGREEMENT
(STANAG)

THE NATO MULTI-CHANNEL TACTICAL DIGITAL GATEWAY - CIRCUIT SWITCHED DATA TRANSMISSION STANDARDS -

Annexes:
A. Definitions
B. Basic Principles
C. Data Communication Formats
D. Application Data Bit Rates and Classes
E. NATO Protocol Implementation Conformance Statement (NPICS) Proforma

Related Documents:

STANAG 4206	-	The NATO Multi-channel Tactical Digital Gateway - System Standards
STANAG 4207	-	The NATO Multi-channel Tactical Digital Gateway - Multiplex Group Framing Standards
STANAG 4208	-	The NATO Multi-channel Tactical Digital Gateway - Signalling Standards
STANAG 4209	-	The NATO Multi-channel Tactical Digital Gateway - Standards for Analogue to Digital Conversion of Speech Signals
STANAG 4210	-	The NATO Multi-channel Tactical Digital Gateway - Cable Link Standards
STANAG 4211	-	The NATO Multi-channel Tactical Digital Gateway - System Control Standards
STANAG 4212	-	The NATO Multi-channel Tactical Digital Gateway - Radio Relay Link Standards
STANAG 4214	-	International Routing and Directory for Tactical Communications Systems
STANAG 4249	-	NATO Reference Model For Open Systems Interconnection
STANAG 5000	-	Interoperability of Tactical Digital Facsimile Equipment
STANAG 5036	-	Parameters and Practices for the Use of the NATO 7-bit code

INTRODUCTION

1. This STANAG is one of a series which, when taken together, specifies all the technical characteristics, parameters and procedures necessary for two NATO tactical digital communications systems (networks) to interconnect and exchange traffic via a gateway.

2. STANAG 4206, the NATO Multi-channel Tactical Digital Gateway - System Standards, provides an overview of the gateway concept and summarizes the key requirements and characteristics contained within this and the other STANAGs of this series.

AIM

3. The aim of this agreement is to define the parameters for non-voice communications on traffic channels over the gateway.

AGREEMENT

4. The participating nations agree to use the characteristics contained in this STANAG as the parameters for non-voice communications on traffic channels between tactical digital systems via a gateway.

GENERAL

5. The requirements and criteria contained herein shall be considered as a minimum.

6. Facilities shall be provided within the automatically switched systems for transmission of non-voice traffic.

IMPLEMENTATION OF THE AGREEMENT

7. The STANAG is implemented by a nation when the multi-channel tactical digital gateways (circuit switched data transmission standards) in that nation's forces comply with the characteristics detailed in this agreement and are placed in service.

DEFINITIONS

a. The term "isochronous signal" is used when the time interval separating any two significant instants (binary state transitions) is theoretically equal to the unit interval or multiples of the unit interval. In practice, variations in the time intervals are required to be within specified limits.

b. The term "anisochronous signal" is used when the time interval separating any two significant instants is not necessarily related to the time interval separating any other two significant instants. For example a unit code operating with a variable 1½ unit stop element and any direct keyboard input from peripherals not equipped for additional bit storage are anisochronous.

c. Two signals are synchronous if their corresponding significant instants have a fixed relationship. In particular, a fixed phase relationship between the transmitted data and the bearer circuit timing is implied.

d. Two signals are asynchronous if their corresponding significant instants do not have a fixed relationship. In particular, a fixed phase relationship between the transmitted data and the bearer circuit timing is not implied.

e. The Data Terminal Equipment (DTE) comprises the data source and/or data sink. It may also include other functions.

f. The Data Circuit Terminating Equipment (DCE) provides all functions required to establish, maintain and terminate a connection, the signal conversion and coding between the DTE and the transmission line. It may also include other functions. Some functions may be realised in other equipment.

g. The term "bearer circuit" is used to describe a transmission circuit. For the purposes of this standard it is the circuit between two DCEs over which data is transported.

ANNEX B to
STANAG 4213
(Edition 3)

BASIC PRINCIPLES

1. Data shall be transmitted via circuit-switched common user circuits having a channel bit rate of 16 kbit/s. Optionally when a higher transmission capacity is required multi-timeslot operation may be used to provide channel bit rates of 32, 48 or 64 kbit/s.
2. Data processing for the purposes of transmission, including error detection/correction to meet the data integrity requirements, shall not be a function of the bearer circuit.

3. Channel-timing in the terminal is not addressed in this STANAG since this is not an issue for interoperability.

4. Facilities shall be provided for direct data communication. The provision of facilities for the indirect communication of data is optional.

5. Subscribers may be provided with a single- or multimode profile DTE (i.e. a subscriber may be provided with more than one type of terminal and/or a terminal may be able to operate in more than one mode). If this is the case then only one terminal and one operating mode shall be used at any one time.

ANNEX C to
STANAG 4213
(Edition 3)

DATA COMMUNICATION FORMATS

DATA CLASSIFICATION

1. The classification of the data type and the respective processing technique that shall be used for transmission over the bearer circuit is shown in Table 1.

Table 1 - Data classification

Class	Data Type Structure	Relationship with Bearer Circuit	Processing Technique
1	Isochronous	Synchronous	None
2	Anisochronous	Asynchronous	Multiple Sampling & Majority Voting, *Note*
3	Isochronous	Asynchronous / Synchronous	Multiple Sampling & Majority Voting with Regeneration, *Note*
4	Isochronous	Synchronous	Forward Error Correction using Block Codes

Note: The method of data processing in the receiver is of local concern as long as performance requirements are met. Majority voting is mentioned here as an example.

DATA BIT RATES

2. Table 2 shows the data bit rates and applied data classes that may be supported and the required bearer circuit bit rate (incl. number of 16 kbit/s timeslots) to support that data bit rate. Also shown is the use of block interleaving.
Table 4 in annex D shows the data bit rates and classes to be used by applications that transfer data over the gateway.

Table 2 - Data bit rates

Data bit rate (kbit/s)	Data class	Bearer circuit bit rate (kbit/s)	Number of timeslots	Block interleaving used: Yes or No
16.0	1	16.0	1	N
0.05 - 2.4	2	16.0	1	N
2.4	3	16.0	1	N
2.4	4	16.0	1	Y
9.6	4	16.0	1	N
32.0	1	32.0	2	N
4.8	4	32.0	2	Y
19.2	4	32.0	2	N
48.0	1	48.0	3	N
64.0	1	64.0	4	N
9.6	4	64.0	4	Y
38.4	4	64.0	4	N

NOTE: not all possible combinations of bit rate and data classes are shown; the table only reflects those combinations that are applicable to (future) existing applications.

DATA PROCESSING

3. The data processing methods for the transmission of the various data types between compatible DTEs shall be as described below.

4. When data processing is performed on bit rates requiring 2, 3 or 4 timeslots, the data processing shall be performed on the resulting bearer circuit bit rate (and not on each individual timeslot).

Note: Paragraphs 5 through 8 address characteristics and operating procedures for single timeslot operation. Multi-timeslot operation is addressed in paragraph 9.

Class 1

5. The block schematic for Class 1 is shown in Figure 1. This figure is meant only as an example for implementation.

5.a The isochronous-synchronous data bit rate for this class shall be 16 kbit/s.

5.b The timing of both the received and transmitted data shall be derived from the bearer circuit.

5.c The received data bit error rate at the DTE is that of the bearer circuit.

Class 2

6. The block schematic for Class 2 is shown in Figure 2. This figure is meant only as an example for implementation.

6.a The anisochronous-asynchronous data bit rates for this class will be in the range 0.05 to 2.4 kbit/s.

6.b The DTE transmitted data is independent of the DCE's timing. It shall be sampled at the bearer circuit bit rate in the DCE before transmission.

6.c The received bearer circuit signal containing the sampled data shall be processed in the receiver, e.g. in a Majority Voting Detector (MVD), so that the performance is as specified in 6.d and 6.e below. (see also paragraph 7.f)

6.d At the data bit rate of 0.05 kbit/s the residual bit error rate after processing will be less than 1 in 10^5 when the random bit error rate on the bearer circuit is equal or less than 1 in 10^2.

6.e At the data bit rate of 2.4 kbit/s the residual bit error rate after processing will be less than 3 in 10^6 when the random bit error rate on the bearer circuit is equal or less than 1 in 10^3.

Class 3

7. The block schematic for Class 3 is shown in Figure 3. This figure is meant only as an example for implementation.

7.a The isochronous-asynchronous/synchronous data bit rate for this class shall be 2.4 kbit/s. For asynchronous operation the tolerance of the data bit rate shall not exceed 1 part in 10^4.

7.b The DTE transmitted data shall be independent of the DCE's timing for asynchronous operation. For synchronous operation the DTE timing shall be under the control of the DCE and shall be derived from the bearer circuit. The DTE transmitted data shall be sampled at the bearer circuit bit rate in the DCE before transmission.

7.c The received bearer circuit signal containing the sampled data shall be processed, e.g. in a MVD, so that the performance is as specified in 7.e below.

7.d The DCE shall recover a 2.4 kbit/s timing signal from the received data signal output and use it to sample the output signal. In order that the DCE shall have recovered a 2.4 kbit/s timing signal prior to the receipt of the data signal, the transmit DTE shall transmit a synchronisation preamble of at least 200 ms. This preamble shall contain at least 25% transitions and there shall not be any gaps between transitions of more than 100 ms. If at any time a pause in traffic at the transmit DTE causes a loss of transitions for 100 ms or more then the synchronisation preamble shall be repeated.

7.e The residual data bit error rate at the DTE will be less than 1 in 10^5 when the bearer circuit random bit error rate is equal to or less than 1 in 10^2.

7.f **Warning:** the definition of class 2 or 3 data transmission is not sufficient to guarantee high integrity data transmission. For this to be achieved the user must employ a higher level checking protocol, i.e. automatic or human interaction, combined with a request for the transmitter to re-send the data (and sync pre-amble for class 3) whenever repeated errors are detected by the receiver.

Class 4

8. The block schematic for Class 4 is shown in Figure 4. This figure is meant only as an example for implementation.

8.a The isochronous-synchronous data bit rates for this class will be 2.4 kbit/s or 9.6 kbit/s.

8.b The DTE timing shall be under the control of the DCE and shall be derived from the bearer circuit. The DCE shall perform the conversion from 16 kbit/s to 9.6 kbit/s and vice versa. For 2.4 kbit/s operation (i.e. 9.6 kbit/s divided by 4) each data bit shall be transmitted four times, by transmitting it in four different blocks (see paragraph 8.p).

8.c The Error Detection Correction (EDC) technique used shall employ the Forward Error Correction (FEC) characteristics of the (31,21) Bose-Chaudhuri-Hocquenghem (BCH) block code, which has the capacity of correcting up to two random errors per block.

8.d In order to reduce the effect of error bursts on the bearer circuit, the BCH blocks may be distributed in the time domain by a process of interleaving (see paragraph 8.p).

8.e At the data bit rate of 2.4 kbit/s the residual data bit error rate at the DTE will be less than 1 in 10^5 when the bearer circuit random bit error rate is equal to or less than 1 in 10^2.

8.f At the data bit rate of 9.6 kbit/s the residual data bit error rate at the DTE will be less than 5.5 in 10^7 when the bearer circuit random bit error rate is equal to or less than 1 in 10^3.

8.g Operating Procedures at 2.4 kbit/s

8.g.1 When operating at a data bit rate of 2.4 kbit/s the data blocks shall be transmitted on a block by block basis using the simple repetition method (i.e. N = 1) or block interleaving method, as described in paragraph 8.p. The same method shall be used in both directions.

8.g.2 The synchronisation procedure shall be as described in paragraph 8.k.

8.g.3 During the traffic state the data block transmissions shall be sent using both the DB1 and DBR data block pattern as described in 8.m.

8.h Operating Procedures at 9.6 kbit/s

8.h.1 When operating at a data bit rate of 9.6 kbit/s it is mandatory that the data blocks be transmitted on a block by block basis.

8.h.2 The synchronisation procedure shall be as described in paragraph 8.k, except that the value of N shall be set to zero in both directions.

8.h.3 During the traffic state all data block transmissions shall be sent using the DB1 data block pattern as described in 8.m.

8.h.4 To reduce the influence of burst errors on the bearer circuit, the implementation of a bit interleaving scheme is for further study.

8.j BCH Block Code

8.j.1 The data to be transmitted shall be coded into a 31 bit block consisting of:
(a) an information field of 21 bits
(b) a polynomial redundancy field of 10 bits

8.j.2 The information field shall be further divided into:
(a) 1 filler bit (set to zero), bit 1
(b) 2 framing bits (F1 and F2), bits 2 and 3
(c) 18 data bits, bits 4 through 21

8.j.3 The information field shall be used to generate the polynomial redundancy bits according to the (31,21) BCH code generator polynomial, G(x)

$$G(x) = (x5 + x2 + 1)\ (x5 + x4 + x3 + x2 + 1)$$

8.j.4 The filler bit (bit 1 of the information field) shall not be transmitted. Thus each transmitted block consists of 30 bits allowing for a data bit rate of

$$\frac{\text{18 bits (data) x 16 kbit/s (channel bit rate)}}{\text{30 bits (transmitted in one block)}} = 9.6 \text{ kbit/s}$$

8.j.5 The block structure is shown below

(31,21) BCH Block Code				
Information Field				Redundancy Field
1	2	3	4 • • • 21	22 • • • 31
0	F1	F2	18 Data Bits	10 Polynomial Bits
	30 Bits Transmitted			

The order of bit transmission of the block is from left to right.

8.k Block Synchronisation Procedure

8.k.1 Prior to the transmission of blocks containing data both DCEs shall perform the block synchronisation procedure. The block synchronisation procedure is shown in the state transition diagram contained in Figure 5. Block interleaving is not performed during the synchronisation procedure.

8.k.2 There are 2 types of synchronisation pattern:
(a) Block Alignment Request (BAR)
(b) Block Alignment Acknowledgement (BAA)

8.k.3 The 2 types of synchronisation pattern shall have the following formats

	F1	F2	8 Bit Sync Pattern	4 Bit Zero	6 Bit N Value	10 Redundancy Bits
BAR	1	1	10010110	0000	Value of N in Binary	Polynomial Bits
BAA	0	1	10010110	0000	Value of N in Binary	Polynomial Bits

8.k.4 The value of N shall be transmitted in binary form as shown below, with the Most Significant Bit (MSB) being transmitted first.

2^5	2^4	2^3	2^2	2^1	2^0
0	X	X	X	X	X

8.k.5 When operating at 9.6 kbit/s the value of N shall be set to zero. When operating at 2.4 kbit/s, N shall be selected in accordance with para 8.p.

8.l Initial Synchronisation

The Initial Synchronisation procedure shall be performed as follows:

a) The synchronisation procedure starts by the transmission of the BAR pattern containing an appropriate value of N (see paragraph 8.p). On receipt of the BAR pattern the DCE shall be adjusted to the received value of N.

b) The DCE shall acknowledge the reception of the BAR pattern and the value of N for the receive direction by transmitting a BAA pattern including a value of N for the opposite direction.

c) If a DCE, that is operating at 2.4 kbit/s, cannot accept the value of N received in the BAR pattern it shall react by transmitting the BAR pattern with the value of N set to 1.

d) A DCE shall enter the traffic state:

1) when a DCE receives the BAA pattern and it has adjusted to the received value of N, while transmitting either the BAR or BAA pattern.
2) when a DCE receives a data block while transmitting the BAA pattern.

8.m Traffic State

8.m.1 When synchronisation is achieved the traffic state shall be entered and followed with the immediate transmission of data blocks.

8.m.2 During the traffic state, to distinguish between the transmission of the first data block of a Multi-Frame and the repetition data blocks the following data block patterns shall be used.

- DB1 for first data block transmission
- DBR for repetition block transmission

	F1	F2	18 Information Bits	10 Redundancy Bits
DB1	0	0	Data	Polynomial Bits
DBR	1	0	Data	Polynomial Bits

8.m.3 The Multi-Frame structure when operating at 2.4 kbit/s interleaved mode shall be as shown in Table 3.

8.m.4 During the traffic state the DCE shall continuously monitor the incoming bit stream for the correct F1/F2 pattern or the BAR pattern. Upon receipt of the BAR pattern, the DCE shall enter the state where it transmits the BAA pattern.

8.n Re-synchronisation

The Re-synchronisation procedure shall be performed as follows:

a) A DCE which has detected the loss of a data block, either Data Block 1 (DB1) or Data Block Repeat (DBR), in the traffic state by detecting loss of F1/F2 pattern , may initiate crypto re-synchronisation when end-to-end encryption is used and shall initiate the transmission of the BAR pattern and shall search for a BAA or BAR pattern according to the rules described in paragraph 8.k

b) A DCE may delay the transmission of the BAR pattern for a time period of 0.5 s ± 20 %, such that if a valid DB1 or DBR is found during this time period no transmission of the BAR pattern shall be initiated. If a valid DB1 or DBR has not been recognised when this time period has expired, then the DCE shall proceed as described in the a) of this paragraph.

c) If during this time period the BAR pattern is received then the DCE shall enter the state in which it transmits the BAA pattern.

8.p Block Interleaving

8.p.1 The efficiency of DTE end-to-end protocols (e.g. HDLC) may be severely affected by any regularity of residual errors at the interface between the DTE and DCE. Such regularity may result from bursts of errors on the bearer circuit. In order to reduce this effect a process of block interleaving when operating at 2.4 kbit/s Class 4 may be applied so as to minimise the probability that more than one of four blocks with identical data will be subjected to burst errors.

8.p.2 The block interleaving process at 2.4 kbit/s shall be performed by constructing a transmission Multi-Frame (MF) of 4N blocks (for the value of N see 8.p.4). The structure of a Multi-Frame and of Multi-Frames is indicated in Table 3.

8.p.3 The order of block transmission is from left to right, line by line (i.e. block 1 - block N with F1 and F2 = 0 followed by 3 x (block 1 - block N) with F1 = 1 and F2 = 0). For F1 and F2 see 8.m.3.

Table 3 - Multi-Frame at 2.4 kbit/s

	F1	F2	Bits 4 - 31 of	F1	F2	Bits 4 - 31 of		F1	F2	Bits 4 - 31 of
	0	0	block 1	0	0	block 2		0	0	block N
MF1	1	0	block 1	1	0	block 2		1	0	block N
	1	0	block 1	1	0	block 2	• •	1	0	block N
	1	0	block 1	1	0	block 2		1	0	block N
MF2	0	0	block (N+1)	0	0	block (N+2)	• •	0	0	block 2N

8.p.4 To reduce the occurrence or erroneous bits being concentrated into individual blocks by errors occurring synchronously with the frame rate, the value of N may be randomly selected during each block synchronisation procedure (see paragraph 8.k).

8.p.5 In order that the contribution of the block interleaving process to the propagation delay shall not normally exceed 200 ms, the mandatory range for the value of N shall be 1 to 15 inclusive. To overcome extreme error conditions and where longer delays are acceptable, higher values of N up to and including a maximum of 31 are optional.

8.p.6 A value of N may be randomly selected during each synchronisation procedure by the source DCE and transmitted to the sink DCE as part of the synchronisation pattern. The value of N for each direction of transmission shall be independently selectable, except for paragraph 8.p.7. below.

8.p.7 To simplify equipment, operation with simple repetition is provided by setting N equal to 1. It is mandatory for the opposite direction upon receiving N equal to 1 also to set its value of N equal to 1 and to simply repeat transmission four times.

8.p.8 When operating at 9.6 kbit/s block interleaving is not applicable and the value of N shall be set to 0.

MULTI-TIMESLOT OPERATION

9. Table 2 specifies bit rates for multi-timeslot operation for classes 1 and 4.

9.a Multi-timeslot operation allows 32, 48 or 64 kbit/s to be sent over a single connection. For switched connections the Connection Request Message shall include the optional channel bit map as specified in Appendix 1, Annex D to STANAG 4208. For permanent connections there shall be bilateral agreement on the application, the number of timeslots and their timeslot numbers.

9.b To ensure end-to-end bit sequence integrity over multi-timeslot connections, the sequence of bits (in each frame) is assigned to timeslots in ascending order, with the first bit placed in the lowest-numbered timeslot. The timeslots assigned are not necessarily consecutive.

Class 1

10. The multi-timeslot data bit rates for this class will be 32, 48 and 64 kbit/s. The bit rates of 32, 48 and 64 kbit/s shall be realised by transmitting the data using 2, 3 or 4 timeslots respectively. The support of multi-timeslot operation is optional.

Class 4

11. The isochronous-synchronous data bit rates for this class will be 4.8 kbit/s or 19.2 kbit/s when using 2 timeslots and 9.6 kbit/s or 38.4 kbit/s when using 4 timeslots. The support of multi-timeslot operation is optional.

11.a Processing

11.a.1 The DTE timing shall be under the control of the DCE and shall be derived from the bearer circuit. The DCE shall perform the conversion from 32 kbit/s to 19.2 kbit/s or from 64 kbit/s to 38.4 kbit/s and vice versa. For 4.8 kbit/s and 9.6 kbit/s (i.e. 19.2 kbit/s divided by 4 and 38.4 kbit/s divided by 4 respectively) each data bit shall be transmitted four times, by transmitting it in four different blocks.

11.a.2 The EDC technique used shall be as for the case of single timeslot operation as specified in 8.c. The BCH Block Code shall be as specified in 8.j.

11.a.3 Block Interleaving may be applied when operating at 4.8 kbit/s using two timeslots or 9.6 kbit/s using four timeslots. The block interleaving process shall be as specified in 8.p.

11.b Synchronisation

11.b.1 The synchronisation procedure shall be performed as specified in paragraphs 8.k through 8.m. using the multi-timeslot connection, i.e. synchronisation will take place at multi-timeslot bit rates.

11.c Operating Procedures at 4.8 kbit/s or 9.6 kbit/s

11.c.1 When operating at a data bit rate of 4.8 kbit/s using two timeslots or 9.6 kbit/s using four timeslots the (31,21) BCH blocks shall be transmitted using the simple repetition method (i.e. N = 1) or block interleaving method, as described in paragraph 8.p. The same method shall be used in both directions.

11.c.2 The synchronisation procedure shall be as described in paragraph 8.k.

11.c.3 During the traffic state the data block transmissions shall be sent using both the DB1 and DBR data block pattern.

11.d Operating Procedures at 19.2 kbit/s or 38.4 kbit/s

11.d.1 When operating at a data bit rate of 19.2 kbit/s using two timeslots or 38.4 kbit/s using four timeslots it is mandatory that the (31,21) BCH blocks be transmitted on a block by block basis.

11.d.2 The synchronisation procedure shall be as described in paragraph 8.k, except that the value of N shall be set to zero in both directions.

11.d.3 During the traffic state all data block transmissions shall be sent using the DB1 data block pattern.

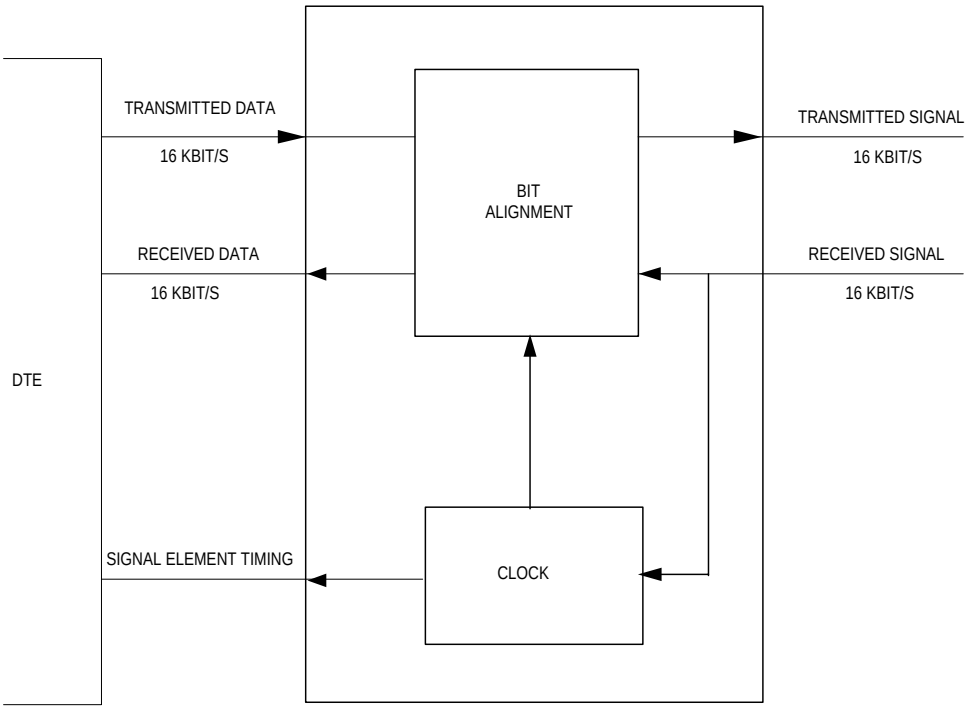


Figure 1 - Block schematic for class 1, example

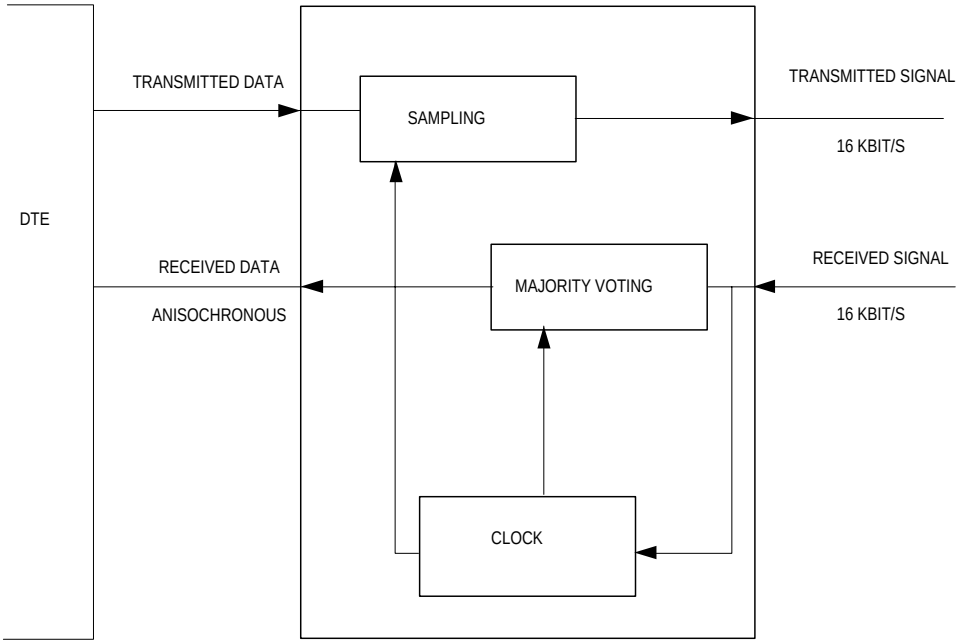


Figure 2 - Block schematic for class 2, example

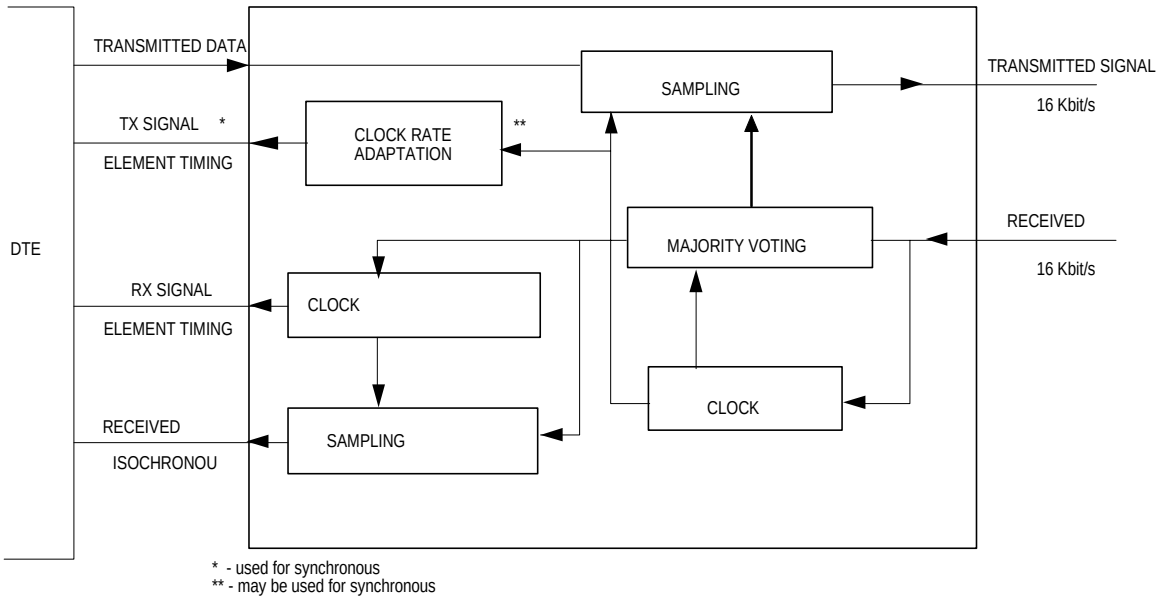


Figure 3 - Block schematic for class 3, example

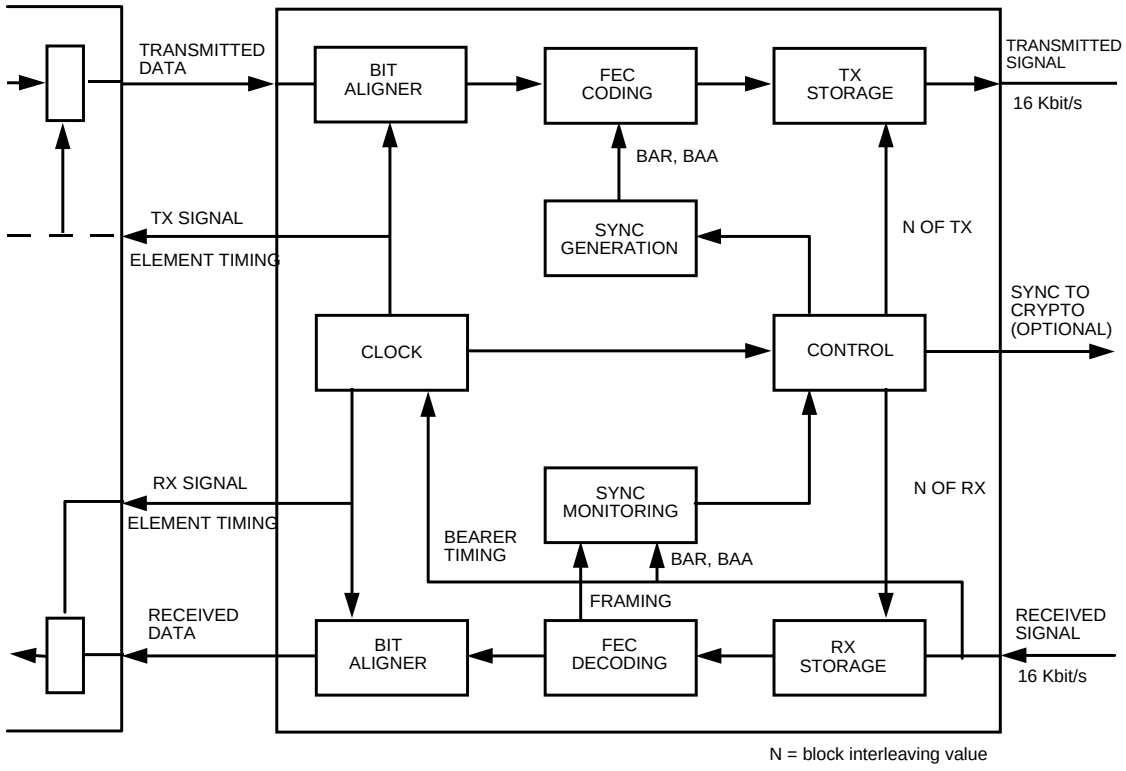


Figure 4 - Block schematic for class 4, example

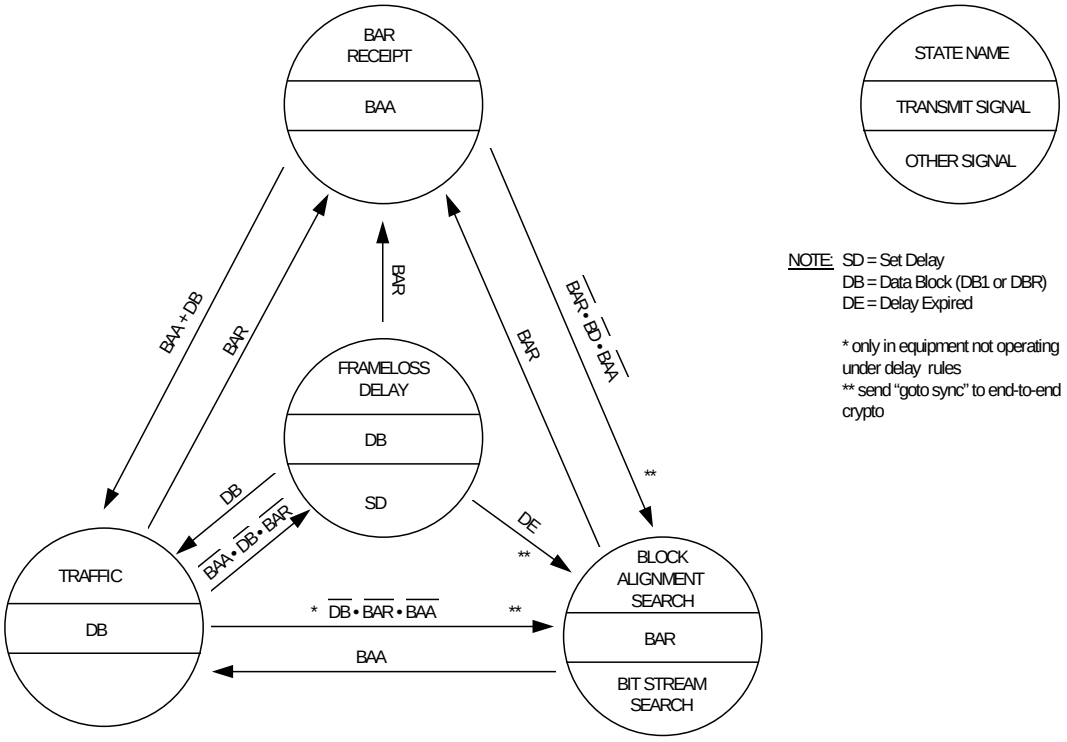


Figure 5 - State-transition diagram

ANNEX D to
STANAG 4213
(Edition 3)

APPLICATION DATA BIT RATES AND CLASSES

1. To ensure interoperability between applications over the gateway the table below specifies the data bit rates and classes to be used by applications.

Table 4 - Application bit rates and classes

Traffic Type	Mode	Class	Bit rate (kbit/s)	Code
Fx	C	1	16.0	*Note 1*
Fx	C	3	2.4	*Note 1*
Tg	C	2	0.05	ITA2
Tg	C	3	2.4	IA5
D *Note 3*	C	1	16.0	*Note 2*
D *Note 3*	C	3	2.4	*Note 2*
D	C	4	2.4	*Note 4*
D	C	4	9.6	*Note 4*
PS	P	4	9.6	*Note 5*

Traffic Type:
Fx = Facsimile
Tg = Telegraphy
D = Data
PS = Packet Switching

Mode:
C = Circuit mode application
P = Packet mode application

Notes:
1. As specified in STANAG 5000.
2. Determined by data terminal equipment.
3. Class 4 is the preferred mode of data transmission.
4. Determined by data terminal equipment and mode of operation.
5. Packet Switching will be overlaid on the Circuit Switched network.

NATO PROTOCOL IMPLEMENTATION CONFORMANCE STATEMENT (NPICS) PROFORMA

1 Introduction

For a protocol implementation which is claimed to conform to STANAG 4213 the following NATO Protocol Implementation Conformance Statement (NPICS) proforma shall be completed.

For a NATO standard, the NPICS corresponds to the Protocol Implementation Conformance Statement (PICS) defined in ISO/IEC 9646-1 for an International Standard. The term NPICS is used to avoid confusion where the requirements for NPICS and PICS differ.

A completed NPICS proforma is the NPICS for the implementation in question. The NPICS is a statement of which capabilities and options of the protocol have been implemented. The NPICS can have a number of uses, including use:

- by the protocol implementor, as a check-list to reduce the risk of failure to conform to the standard through oversight;

- by the supplier and acquirer - or potential acquirer - of the implementation, as a detailed indication of the capabilities of the implementation, stated relative to the common basis for understanding provided by the standard NPICS proforma;

- by the user - or potential user - of the implementation, as a basis for initially checking the possibility of interworking with another implementation (note that, while interworking can never be guaranteed, failure to interwork can often be predicted from incompatible NPICSs);

- by a protocol tester, as the basis for selecting appropriate tests against which to assess the claim for conformance of the implementation.

Note E.1: All material in the base standard, i.e. STANAG 4213, is considered mandatory unless another status is specifically indicated in this NPICS Proforma.

2 Abbreviations and special symbols

2.1 Status symbols

M	mandatory
O	optional
O.<n>	optional, but support of at least one, or exactly one, of the group of options labeled by the same numeral <n> is required
X	prohibited
<pred>:	conditional-item symbol, including predicate identification, see 3.4
¬	logical negation, applied to a conditional item's predicate

2.2 General abbreviations

D	Data
DCE	Data Circuit-terminating Equipment
FEC	Forward Error Correction
Fx	Facsimile
N/A	Not Applicable
S&F	Store and Forward
TG	Telegraphy

2.3 Item references

Items in the NPICS proforma are identified by mnemonic item references. NPICS items dealing with related functions are identified by item references sharing the same initial letter or letter sequence (in capitals). There follows a list of those initials, in the order in which the groups of items occur in the NPICS proforma.

K	bit rate (kbit/s)
C	data Class
RC	combination of bit Rate and data Class
MO	Multi-timeslot Operation
C1T	Class 1 Transmit
C2T	Class 2 Transmit
C2R	Class 2 Receive
C3T	Class 3 Transmit
C3R	Class 3 Receive
C4T	Class 4 Transmission
BI	Block Interleaving
EC	Error Correction
BS	Block Synchronization
MF	Multi-Frame
SR	Simple Repetition
VN	Value of N
M4	Multi-timeslot class 4
M4T	Multi-timeslot class 4 Transmission

MB	Multi-timeslot with Block interleaving
MS	Multi-timeslot Synchronisation
FX	Facsimile
TG	Telegraphy
D	Data
PS	Packet Switching

2.4 Base Standard References

The generic format of a reference of the NPICS proforma is:

<Paragraph>

for a reference to main STANAG part, and

[<Part>]<Annex>[<Appendix>]/<Paragraph>

for all other STANAG references.

<Part>	= A capital Roman number	(I, II, etc.)
<Annex>	= An uppercase letter	(A, B, etc.)
<Appendix>	= A number or uppercase letter	(A, B, etc., 1, 2, etc.)
<Paragraph>	= <n>.[<n>] or <n>.[<x>] as appropriate	
[ ]	enclose an optional entry	
<>	denote a generic identifier	
<n>	A numeral (1, 2, 3 etc.)	
<x>	A lowercase letter (a, b, c etc.)	

In the case when there are references to one or more ITU or ISO base standards in addition to STANAG references, the STANAG references shall be prefixed by "STxxxx", while the ITU or ISO references are direct to chapters, paragraphs etc. Such ITU or ISO base standards shall be listed in the "Related Documents"-sections of this STANAG or STANAG Annex, to which this PICS Proforma is attached. If more than one ITU or ISO standard is referenced in the NPICS Proforma, only one reference should be used in each table, with the reference stated above the table.

3 Instructions for completing the NPICS proforma

3.1 General Structure of the NPICS Proforma

The first part of the NPICS proforma - Implementation Identification and Protocol

Summary - is to be completed as indicated with the information necessary to identify fully both the supplier and the implementation.

The main part of the NPICS proforma is a fixed-format questionnaire, divided into a number of major subclauses; these can be divided into further subclauses each containing a group of individual items. Answers to the questionnaire items are to be provided in the rightmost column, either by simply marking an answer to indicate a restricted choice (usually Yes or No), or by entering a value or a set or range of values. There are some items where two or more choices from a set of possible answers can apply: all relevant choices are to be marked.

Each item is identified by an item reference in the first column; the second column contains the question to be answered; the third column contains the reference or references to STANAG 4213 according to 2.4 above. The remaining columns record the status of the item - whether support is mandatory, optional, prohibited or conditional - and provide the space for the answers: see also 3.4 below.

A supplier may also provide - or be required to provide - further information, categorized as either Additional Information or Exception Information. When present, each kind of further information is to be provided in a further subclause of items labeled A<i> or X<i> respectively for cross-referencing purposes, where <i> is any unambiguous identification for the item (e.g. simply a numeral): there are no other restrictions on its format and presentation.

A completed NPICS proforma, including any Additional Information and Exception Information, is the NATO Protocol Implementation Conformance Statement for the implementation in question.

Note E.2: Where an implementation is capable of being configured in more than one way, a single NPICS may be able to describe all such configurations. However, the supplier has the choice of providing more than one NPICS, each covering some subset of the implementation's configuration capabilities, in case that makes for easier and clearer presentation of the information.

3.2 Additional Information

Items of Additional Information allow a supplier to provide additional information intended to assist the interpretation of the NPICS. It is not intended or expected that a large quantity will be supplied, and an NPICS can be considered complete without any such information. Examples might be an outline of the ways in which a (single) implementation can be set up to operate in a variety of environments and configurations; or a brief rationale - based perhaps upon specific application needs - for the exclusion of

features which, although optional, are nonetheless commonly present in implementations of this protocol.

References to items of Additional Information may be entered next to any answer in the questionnaire, and may be included in items of Exception Information.

3.3 Exception Information

It may occasionally happen that a supplier will wish to answer an item with mandatory or prohibited status (after any conditions have been applied) in a way that conflicts with the indicated requirement. No pre-printed answer will be found in the Support column for this: instead, the supplier shall write the missing answer into the Support column, together with an X<i> reference to an item of Exception Information, and shall provide the appropriate rationale in the Exception item itself.

An implementation for which an Exception item is required in this way does not conform to STANAG 4213.

Note E.3: A possible reason for the situation described above is that a defect in the standard has been reported, a correction for which is expected to change the requirement not met by the implementation.

3.4 Conditional status

3.4.1 Conditional items

The NPICS proforma contains a number of conditional items. These are items for which the status - mandatory, optional or prohibited - that applies is dependent upon whether or not certain other items are supported, or upon the values supported for other items.

In many cases, whether or not the item applies at all is conditional in this way, as well as the status when the item does apply.

Where a group of items is subject to the same condition for applicability, a separate preliminary question about the condition appears at the head of the group, with an instruction to skip to a later point in the questionnaire if the "Not Applicable" answer is selected. Otherwise, individual conditional items are indicated by one or more conditional symbols (on separate lines) in the status column.

A conditional symbol is of the form "<pred>:<x>" where "<pred>" is a predicate as described in 3.4.2 below, and "<x>" is one of the status symbols M, O, O.<n> or X.

If the value of the predicate in any line of a conditional item is true (see 3.4.2), the conditional item is applicable, and its status is that indicated by the status symbol following the predicate; the answer column is to be marked in the usual way. If the value of a predicate is false, the Not Applicable (N/A) answer is to be marked in the relevant line. Each line in a multi-line conditional item should be marked.

3.4.2 Predicates

A predicate is one of the following:

a) an item-reference for an item in the NPICS proforma: the value of the predicate is true if the item is marked as supported, and is false otherwise; or

b) a predicate name, for a predicate defined elsewhere in the NPICS proforma item: see below; or

c) the logical negation symbol "¬" prefixed to an item-reference or predicate name; the value of the predicate is true if the value of the predicate formed by omitting the "¬" is false, and vice versa.

The definition for a predicate name is a Boolean expression constructed by combining simple predicates, as at a) or b) above, using the Boolean operators AND, OR and NOT, and parentheses, in the usual way. The value of such a predicate is true if the Boolean expression evaluates to true when the item-references are interpreted as at a) above.

Each item whose reference is used in a predicate or predicate definition is indicated by an asterisk in the Item column.

4 Identification

4.1 Implementation identification

Nation/Supplier	
Contact point for queries about the NPICS	
Implementation Name(s) and Version(s)	
Other information necessary for full identification - e.g. name(s) and version(s) of machines and/or operating systems; system names	

Notes:
1. Only the first three items are required for all implementations; other information may be completed as appropriate in meeting the requirement for full identification.
2. The terms Name and Version should be interpreted appropriately to correspond with a nation/supplier's terminology (e.g. Type, Series, Model).

4.2 Protocol identification

Identification of protocol specification	STANAG 4213	
Identification of amendments and corrigenda to this NPICS proforma which have been completed as part of this NPICS	Am. : Corr. : Am. : Corr. : Am. : Corr. : Am. : Corr. :	
Have any Exception items been required (see 3.3)? (The answer Yes means that the implementation does not conform to STANAG 4213)		No[] Yes[]

Date of Statement	

5 Implementation

5.1 General Characteristics

Item	Protocol feature	Reference	Status	Support
	Channel bit rate:			
K16	16 kbit/s	B/1	M	Y[]
K32	32 kbit/s using multi-timeslot operation	B/1	O	Y[] N[]
K48	48 kbit/s using multi-timeslot operation	B/1	O	Y[] N[]
K64	64 kbit/s using multi-timeslot operation	B/1	O	Y[] N[]
	Supported data classes:			
C1	Class 1	C/1 table 1	O.1	Y[] N[]
C2	Class 2	C/1 table 1	O.1	Y[] N[]
C3	Class 3	C/1 table 1	O.1	Y[] N[]
C4	Class 4	C/1 table 1	O.1	Y[] N[]
	Combinations of bit rate and data classes supported across the gateway			
RC1	If Class 1 is not supported mark N/A and continue at RC2			N/A[]
RC1a	16 kbit/s Class 1	C/2 table 2, C/5.a	M	Y[]
RC1b	32 kbit/s Class 1	C/2 table 2, C/10	O	Y[] N[]
RC1c	48 kbit/s Class 1	C/2 table 2, C/10	O	Y[] N[]
RC1d	64 kbit/s Class 1	C/2 table 2, C/10	O	Y[] N[]
*RC2	If Class 2 is not supported mark N/A and continue at RC3			N/A[]
RC2a	50 bit/s Class 2	C/2 table 2, C/6,a	O.2	Y[] N[]
RC2b	75 bit/s Class 2	C/2 table 2, C/6,a	O.2	Y[] N[]
RC2c	100 bit/s Class 2	C/2 table 2, C/6,a	O.2	Y[] N[]
RC2d	110 bit/s Class 2	C/2 table 2, C/6,a	O.2	Y[] N[]
RC2e	150 bit/s Class 2	C/2 table 2, C/6,a	O.2	Y[] N[]
RC2f	200 bit/s Class 2	C/2 table 2, C/6,a	O.2	Y[] N[]
RC2g	300 bit/s Class 2	C/2 table 2, C/6,a	O.2	Y[] N[]
RC2h	600 bit/s Class 2	C/2 table 2, C/6,a	O.2	Y[] N[]
RC2j	1200 bit/s Class 2	C/2 table 2, C/6,a	O.2	Y[] N[]
RC2k	2400 bit/s Class 2	C/2 table 2, C/6,a	O.2	Y[] N[]
*RC3	If Class 3 is not supported mark N/A and continue at RC4			N/A[]
RC3a	2.4 kbit/s Class 3	C/2 table 2, C/7.a	M	Y[]
*RC4	If Class 4 is not supported mark N/A and continue at MO			N/A[]
*RC4a	2.4 kbit/s Class 4	C/2 table 2, C/8.a	O	Y[] N[]
*RC4b	4.8 kbit/s Class 4	C/2 table 2, C/11	O	Y[] N[]
*RC4c	9.6 kbit/s Class 4	C/2 table 2, C/8.a	O	Y[] N[]
*RC4d	9.6 kbit/s Class 4, with block interleaving	C/2 table 2, C/11	O	Y[] N[]
*RC4e	19.2 kbit/s Class 4	C/2 table 2, C/11	O	Y[] N[]
*RC4f	38.4 kbit/s Class 4	C/2 table 2, C/11	O	Y[] N[]

RC4a is used in items BIa and BIb
RC4b is used in items Mba and Mbb and in para 5.5.1
RC4c is used in item BSb
RC4d is used in items MBb and MBd and in para 5.5.1
RC4e is used in item MSb and in para 5.5.1
RC4f is used in item MSc and in para 5.5.1

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5.1 continued

	MULTI-TIMESLOT OPERATION			
MO	If multi-timeslot operation is not supported mark N/A and continue at 5.2			N/A[]
Moa	For switched connections does the Connection Request Message include the channel bit map as specified in STANAG 4208?	C/9.a	M	Y[]
Mob	Is sequence if bits in each frame assigned to timeslots in ascending order?	C/9.b	M	Y[]

5.2 Class 1 Data

If Class 1 data service is not supported i.e. Item RC1 mark N/A and continue at 5.3 N/A [ ]

Item	Protocol feature	Reference	Status	Support
C1T	Is the transmit side timing derived from the bearer circuit ?	C/5.b	M	Y[]

5.3 Class 2 Data

If Class 2 data service is not supported i.e. Item RC2, mark N/A and continue at 5.4 N/A [ ]

Item	Protocol feature	Reference	Status	Support
C2T	Is the data to be transmitted sampled at the bearer rate?	C/6.b	M	Y[]
C2R	Is the received bearer circuit signal processed so that specified performance is achieved?	C/6.b, c, d	M	Y[]

5.4 Class 3 Data

If Class 3 data service is not supported i.e. Item RC3, mark N/A and continue at 5.5 N/A [ ]

Item	Protocol feature	Reference	Status	Support
C3Ta	Is the tolerance on asynchronous data within 1 part in 10e4?	C/7.a	M	Y[]
C3Tb	Is the data to be transmitted sampled at the bearer rate?	C/7.b	M	Y[]
C3Tc	Does transmission start with a synchronisation preamble conforming to the specifications?	C/7.d	M	Y[]
C3R	Is the received bearer circuit signal processed so that specified performance is achieved?	C/7.c, C/7.e	M	Y[]

5.5 Class 4 Data

If Class 4 data service is not supported i.e. Item RC4 mark N/A and continue at 5.6 N/A [ ]

Item	Protocol feature	Reference	Status	Support
	TRANSMISSION			
C4Ta	Is data transmission performed on a block-by-block basis?	C/8.g.1, C/8.h.1	M	Y[]
C4Tb	Do the transmitted blocks conform to the BCH specifications in reference?	C/8.j, C/8.k.3, C/8.m.2	M	Y[]
BIa	At 2.4 kbit/s is block interleaving supported as simple repetition	C/8.g.1, C/8.p.7	RC4a:M	N/A[] Y[]

	(N=1)?			
*BIb	At 2.4 kbit/s is block interleaving supported with N>1 as described in para 8.p?	C/8.g.1	RC4a:O	N/A[] Y[] N[]

BIb is used in lines Vna, VNb and VNc

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5.5 continued

	ERROR CONTROL			
EC	Does the EDC technique use the FEC, based on the (31,21) BCH code generator polynomial?	C/8.j.3	M	Y[]
	SYNCHRONISATION			
BSa	Does the synchronisation procedure conform to the state transition diagram in reference?	C/fig. 5	M	Y[]
BSb	Is the value of N in BAR and BAA set to 0 for operation at 9.6 kbit/s?	C/8.k.5, C/8.p.8	RC4c:M	N/A[] Y[]
BSc	Is the transmission of (re)synchronisation pattern delayed by the DCE?	C/8.n.b	O	Y[] N[]
	BLOCK INTERLEAVING FOR CLASS 4 AT 2.4 KBIT/S			
BI	If Block Interleaving is not supported mark N/A and continue at 5.5.1			N/A[]
MF	Is block interleaving performed by constructing a Multi-Frame?	C/8.p.2, table 3	M	Y[]
SR	If N=1 for one direction, does N=1 for the other direction?	C/8.p.7	M	Y[]
VNa	Are all values of N from 1 to 15 inclusive supported in both transmission directions?	C/8.p.5	BIb:M	N/A[] Y[]
VNb	Are values higher than 15 up to and including 31 supported?	C/8.p.5	BIb:O	N/A[] Y[] N[] Nmax:[ ]
VNc	Except for N=1, is the value of N independently selectable for each direction of transmission?	C/8.p.6	BIb:M	N/A[] Y[]

5.5.1 Multi-timeslot Class 4 Data

If multi-timeslot Class 4 data service is not supported i.e. Items RC4b, d, e and f mark N/A and skip this table N/A [ ]

Item	Protocol feature	Reference	Status	Support
M4	Is data processing on multi-timeslot bit rates performed on resulting bearer circuit bit rate?	C/4	M	Y[]
	TRANSMISSION			
M4T	Is data transmission performed on a block-by-block basis?	C/11.c.1, C/11.d.1	M	Y[]
MBa	At 4.8 kbit/s using two timeslots is block interleaving supported as simple repetition (N=1)?	C/11.c.1	RC4b:M	N/A[]Y[]
MBb	At 9.6 kbit/s using four timeslots, is block interleaving supported as simple repetition (N=1)?	C/11.c.1	RC4d:M	N/A[]Y[]
MBc	At 4.8 kbit/s using two timeslots is block interleaving supported with N>1 as described in para 8.p?	C/11.a.4, C/11.c.1	RC4b:O	N/A[]Y[] N[]
MBd	At 9.6 kbit/s using four timeslots, is block interleaving supported with N>1 as described in para 8.p?	C/11.a.4, C/11.c.1	RC4d:O	N/A[]Y[] N[]
	SYNCHRONISATION			
MSa	Is the synchronisation procedure carried out at multi-timeslot bit rates?	C/11.b.1	M	Y[]
MSb	Is the value of N in BAR and BAA set to 0 for operation at 19.2 kbit/s using two timeslots?	C/11.d.2	RC4e:M	N/A[]Y[]
MSc	Is the value of N in BAR and BAA set to 0 for operation at 38.4 kbit/s using four timeslots?	C/11.d.2	RC4f:M	N/A[]Y[]

5.6 Application Data Bit Rates and Classes

Item	Protocol feature	Reference	Status	Support
	SUPPORTED APPLICATIONS			
*FX	Is Facsimile supported over the gateway?	D table 4	O	Y[] N[]
*TG	Is Telegraphy supported over the gateway?	D table 4	O	Y[] N[]
*D	Is Data supported over the gateway?	D table 4	O	Y[] N[]
*PS	Is Packet Switching supported over the gateway?	D table 4	O	Y[] N[]
	BIT RATE AND CLASS USED OVER THE GATEWAY			
FX1	Is Facsimile transferred using 16 kbit/s class 1 transmission?	D table 4	FX:O	N/A[] Y[] N[]
FX2	Is Facsimile transferred using 2.4 kbit/s class 3 transmission?	D table 4	FX:M	N/A[] Y[] N[]
TG1	Is Telegraphy transferred using 50 bit/s class 2 transmission?	D table 4	TG:M	N/A[] Y[] N[]
TG2	Is Telegraphy transferred using 2.4 kbit/s class 3 transmission?	D table 4	TG:O	N/A[] Y[] N[]
D1	Can Data be transferred using 16 kbit/s class 1 transmission?	D table 4	D:O	N/A[] Y[] N[]
D2	Can Data be transferred using 2.4 kbit/s class 3 transmission?	D table 4	D:O	N/A[] Y[] N[]
D3	Can Data be transferred using 2.4 kbit/s class 4 transmission?	D table 4	D:M	N/A[] Y[]
D4	Can Data be transferred using 9.6 kbit/s class 4 transmission?	D table 4	D:O	N/A[] Y[] N[]
PS1	Is Packet Switching supported with 9.6 kbit/s class 4 channels?	D table 4	PS:M	N/A[] Y[]